12-kW *S*-Band Solid-State Transmitter for Modern Radar Systems

Michael Hanczor, *Member, IEEE,* and Mahesh Kumar, *Senior Member, IEEE*

***Abstract*—This paper presents the development of a 12-kW solid-state transmitter, operating over 2.7–2.9 GHz, used in modern surveillance and air-traffic control (i.e., MATCALS AN/TPS-73) radars. 12 kW of peak power with a pulse width of 100 μs and duty cycle of 10 percent is achieved by combining 56 300 W high-power solid-state amplifiers. Other key performance parameters are pulse-to-pulse stability (MTI improvement factor of >90 dB), MTBF of >22 000 h, instantaneous bandwidth of 200 MHz, extremely high pulse fidelity and self-pulsing low-voltage operation for high efficiency.**

I. Introduction

MOST RADAR systems currently use TWT/Klystron transmitters. Modern and future radar systems require performance that cannot be achieved by these tube-type transmitters. For a TWT/Klystron transmitter, the MTI improvement factor is ~60 dB, MTBF ~5000 h, instantaneous bandwidths of up to 10 percent, and the voltages required are 45–80 kV, which are extremely difficult to regulate [1].

A 12-kW solid-state transmitter (SST) is developed to overcome the limitations of tube-type transmitters. The development of the MATCALS AN/TPS-73 transmitter presented in this paper achieves the following key performance parameters: MTI improvement factor of >90 dB, MTBF >22 000 h, instantaneous bandwidth of >200 MHz, low voltage (36 V) self-pulsing operation yielding high efficiency, maximum transistor junction temperature <125°C.

The output power of 12 kW is achieved by combining 56 300 W amplifiers using four 14:1 reactive radial combiners. The architecture of the transmitter design is such that amplifier modules can be serviced while maintaining the continuous operation of the transmitter.

The 12-kW SST has successfully completed all environmental stress and screen (ESS) system tests and is presently in full-scale production. This stand-alone SST developed for the marine air-traffice control and landing system (MATCALS) AN/TPS-73 is currently the first and only *S*-band SST operating in the field.

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The authors are with the Unisys Government Systems Group, Great Neck, NY 11020.

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II. Transmitter Design

A block diagram of the 12-kW solid-state transmitter (SST) is shown in Fig. 1. The overall gain of the SST is 29 dB, which is achieved by three stages of amplification. The outputs of the first and second stage amplifiers are 85 and 300 W, respectively. The output stage consists of 56 300-W amplifiers (HPA's) that are combined in four quadrants. Each quadrant produces 3.5 kW output power. The 3.5-kW amplifier consists of 14 300-W HPA's combined using a 14:1 reactive, center fed, stripline combiner network in a radial configuration. The four 3.5 kW amplifiers are combined using a 4:1 waveguide combiner to produce an output power of 12 kW.

As shown in Fig. 1, the first and second stages are designed to provide full redundancy by automatic switching to alternate standby amplifiers, when the operating amplifier exhibits failure or reduced output power. Quadrant switching is also provided to produce output powers of 0.75, 1.5, 3, 6, and 12 kW for multiple mission requirements. This special feature also gives the flexibility to service and maintain any quadrant while the system is in operation.

III. 300- and 85-W Amplifier Designs

The heart of the solid-state transmitter is the solid-state high-power amplifier (HPA). The *S*-Band HPA design began with the selection of an architecture to meet the overall power, gain, efficiency, and thermal requirements. The circuit topology is chosen based on the availability of the *S*-band power transistor such that the minimum number of transistors are required to be combined to provide overall output power for the HPA [2]. This is important since the loss in the combiner increases with the number of transistors to be combined. The efficiency of the high-power transistor is inversely proportional to the output power, since many cells are combined within a transistor to provide the required output power.

A block diagram of the 300-W HPA is shown in Fig. 2. The architecture for the HPA consists of three stages of amplification that amplifies a 5-W input signal to a 300-W output signal [3]. The first stage is a 20-W power transistor that supplies 17-W minimum to the second stage. The second stage transistor is an 85-W device having a minimum gain of 6.5 dB followed by a third stage of four paralleled 85-W transistors, as seen in Fig. 2. A transistor with an output power of 85 W is selected to be combined

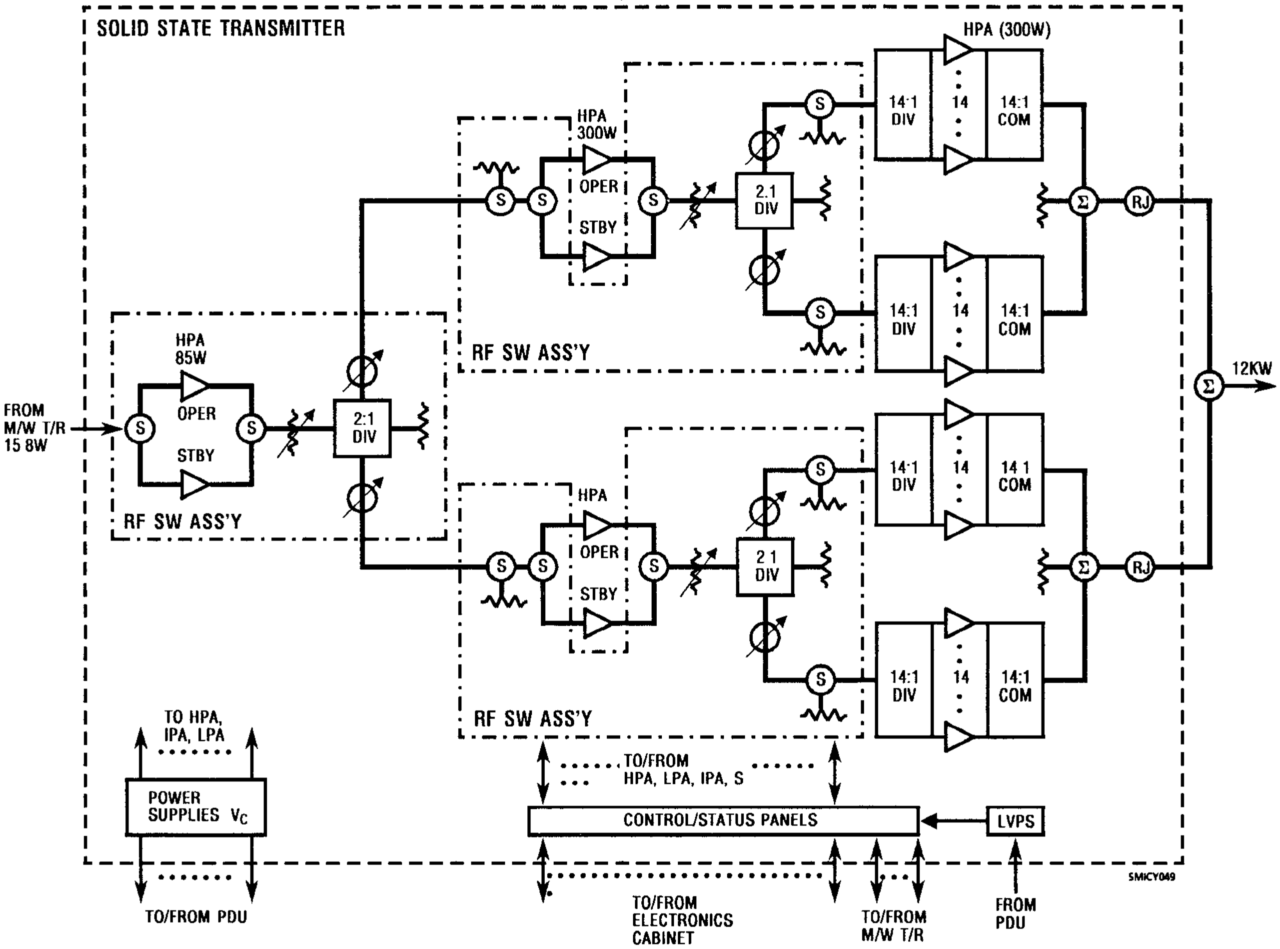

Fig. 1. Solid-state transmitter block diagram.

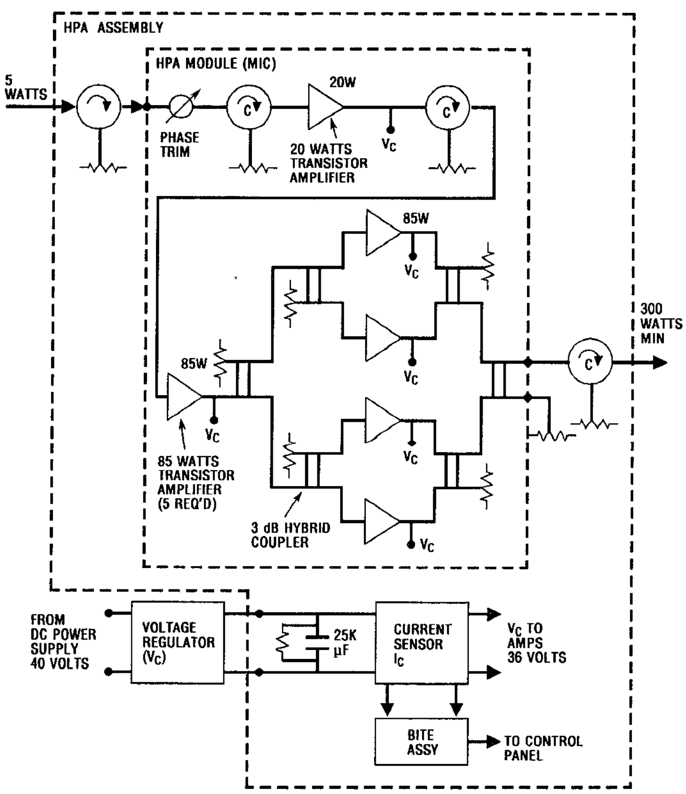

Fig. 2. HPA assembly block diagram.

in a four-way combiner to obtain 300-W output power. A four-way power divider/combiner consisting of two levels of two-branch branchline microstrip couplers is used to excite and collect power from the four parallel output stage transistors.

The four-way power divider/combiner provides a good match, good isolation, and low loss. Extreme care was taken to minimize the impedance mismatch of the cascaded MIC circuitry to the output of the final stages. A circulator is used on the output of the HPA module to maintain a constant load VSWR. Further isolation from load VSWR variations is provided by the power combiner. At the input four-way power divider the hybrid branchline couplers provide an input match (output match of second stage) that is degraded only by the isolation of the couplers when the four output ports are terminated in equal mismatches [4]. Reflected power is terminated in the terminations of the isolated ports of the hybrid couplers.

The HPA module contains an input isolator and an isolator between the first and second stage. These isolators are very low loss (<0.2 dB), which were designed as above resonance units to handle various levels of peak power without performance degradation. The isolator between the first and second stage provides interstage isolation of at least 25 dB. The isolator at the input of the

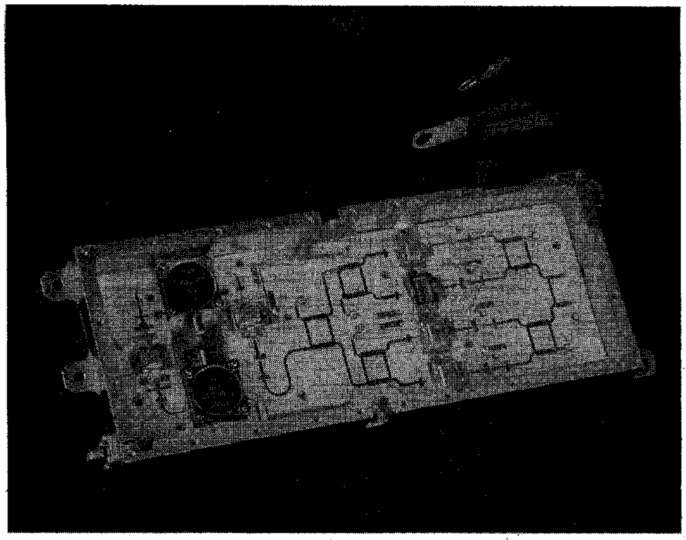

Fig. 3. Photograph of 300-W S-band solid-state high-power amplifiers.

TABLE I
HPA PERFORMANCE

Frequency	2.7 to 2.9 GHz
Pulse width	100 μs and 10 μs
Duty cycle	11 percent
Output power	300 W peak minimum
Input power	5 W peak
Gain	17 dB minimum
Collector voltage	36 V (amplifier)
	39.5 V (regulator)
Collector current	3.6 A (average)
	(regulator input)
Efficiency	26 percent
$\Delta P_o/\Delta V_{cc}$	0.2 dB/V
$\Delta\Phi/\Delta V_{cc}$	4.5°/V
V_{cc} regulation	3 mV
Unit to Unit Tracking	
Amplitude	0.5 dB RMS
Phase	10° RMS

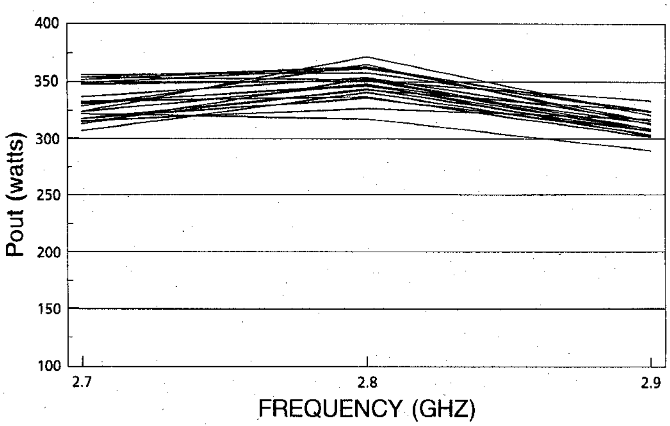

Fig. 4. Variation of output power of 20 S-band 300-W HPA's as a function of frequency.

first stage provides isolation from mismatches of the loaded line phase shifters (see Fig. 2) that are used to phase track HPA modules in the solid-state transmitter.

A photograph of the 300-W HPA module is shown in Fig. 3. The performance of 300-W HPA is presented in Table I. The output power and efficiency of a representative sample of production high-power amplifiers are presented in Figs. 4 and 5, respectively.

The 85-W low-power amplifier (LPA) consists of the first two stages of the 300-W HPA, as shown in Fig. 2.

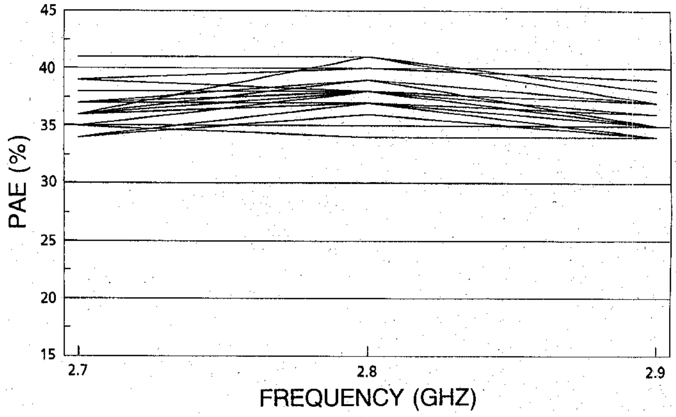

Fig. 5. Variation of power added frequency of 20 300-W HPA's as a function of frequency.

IV. Transistor Development

A high-power silicon bipolar NPN transistor specifically needed for S-band high-power amplifiers was developed. The transistor is a 12-cell device with peak output power of 85 W at 100 μs pulse width and 11 percent duty cycle over a 2.7–2.9 GHz bandwidth. The device was specifically designed to operate with a maximum flange to junction temperature rise (ΔT_{jf}) of 70°C. A low RF thermal resistance was achieved with a transistor chip that has a high-density overlay geometry with emitter site ballasting [5]. The 12 cells of the transistor were internally matched, using bondwires as inductors and MOS capacitors, in an MSC AMPAC* package to provide an input/output impedances of $\sim$5–15 Ω. A photograph of the transistor is shown in Fig. 6. Table II lists the characteristics of this transistor.

V. 14 : 1 Power Combiner Design

The 14 : 1 power combiner is a center fed, reactive, air dielectric stripline combiner using maximally flat, two-transformer sections [4]. The RF schematic of the 14 : 1 combiner is shown in Fig. 7. The 14 50-Ω ports are first combined in pairs, setting up several lines each at a 25-Ω level. The 25-Ω ohm lines are transformed up to 350 ohms through the two-section maximally flat transformer. The seven parallel 350-Ω lines provide a 50-Ω ohm input at the summing point, thereby achieving an impedance match to 50 ohms. A layout of the 14 : 1 combiner is shown in Fig. 8. A coupling to anyone of the 14 output/input ports of 11.8 ± 0.2 dB is achieved with maximum insertion loss of 0.35 dB, a VSWR of less than 1.2 : 1, an isolation of 18 dB and phase variations of less than ±6°.

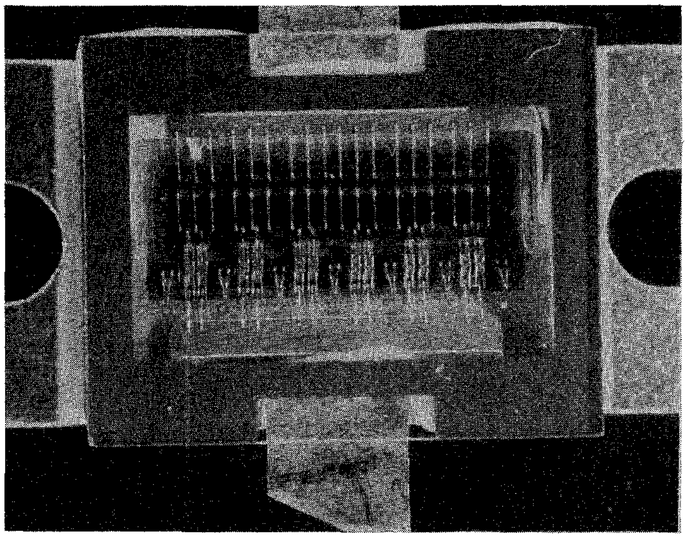

Fig. 6. Photograph of an 85-W S-band transistor.

TABLE II
ELECTRICAL CHARATERISTICS OF 85-W TRANSISTOR

Frequency	2.7 to 2.9 GHz
Output power	85 W peak minimum
Pulse width	100 μs
Duty cycle	11 percent
Collector voltage	36 V
Gain	6.5 dB minimum
Collector efficiency	40 percent minimum
Pulse droop	0.3 dB maximum
$\Delta\Phi/\Delta V_{cc}$	4.5 deg/V max
$\Delta P_o/\Delta V_{cc}$	0.4 dB/V

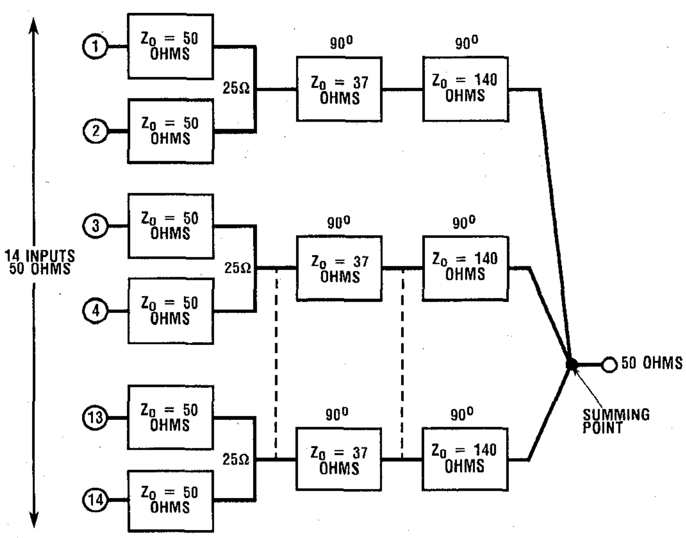

Fig. 7. Schematic of 14 : 1 power divider/combiner.

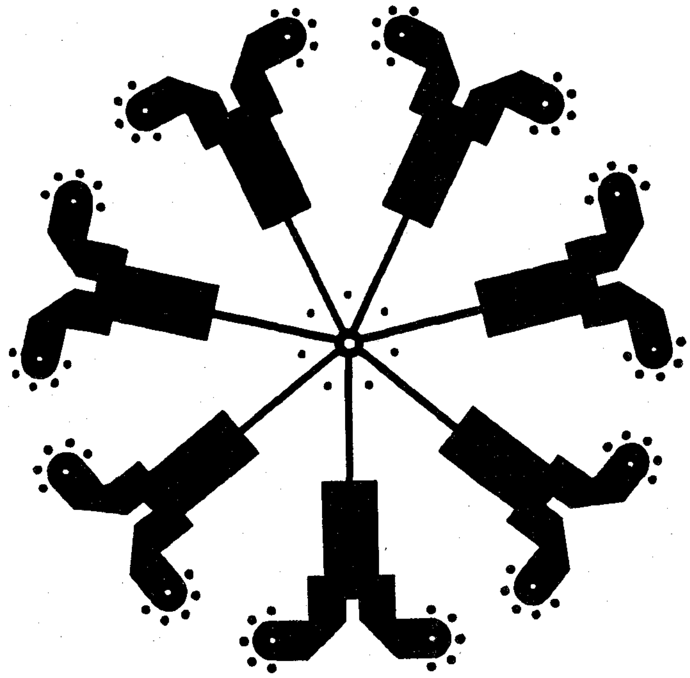

Fig. 8. Layout of 14 : 1 power divider/combiner stripline circuit.

VI. MTI Improvement Factor Calculation

The amplitude and phase instability in a train of output RF pulses place an upper limit on the MTI improvement factor that can be realized in a radar system [1]. The limiting improvement factor due to phase instability and amplitude instability are

$$I = 20 \log \left(\frac{1}{\Delta\Phi}\right) \quad \Delta\Phi = \begin{array}{l}\text{interpulse phase change} \\ \text{(radians)}\end{array} \tag{1}$$

$$I = 20 \log \left(\frac{A}{\Delta A}\right) \quad \begin{array}{l} A = \text{amplitude (volts)} \\ \Delta A = \text{amplitude change}\end{array} \tag{2}$$

The measured phase and amplitude pushing factors for a 300-W HPA were

$$\frac{\Delta\Phi}{\Delta V_{cc}} = \leq 5^\circ/\text{V} \tag{3}$$

$$\frac{\Delta P_o}{\Delta V_{cc}} = \leq 0.5 \text{ dB/V} \tag{4}$$

With a 3-mV regulation obtained from the voltage regulator and pushing factors values shown in (3) and (4), the calculated combined MTI improvement factor for the 300-W HPA due to amplitude and phase instabilities is 76 dB.

The MIT improvement factor for the transmitter consisting of N amplifiers in the output stage is

$$\text{MTI improvement factor for transmitter for HPA} + 10 \log N = \text{MTI improvement factor} \tag{5}$$

Therefore, for the 12-kW transmitter with 56 amplifiers, the calculated MTI improvement factor is 93 dB.

VII. SST Fabrication

The solid-state transmitter shown in Fig. 9 develops 12 kW of output power from 56 high-power amplifiers ar-

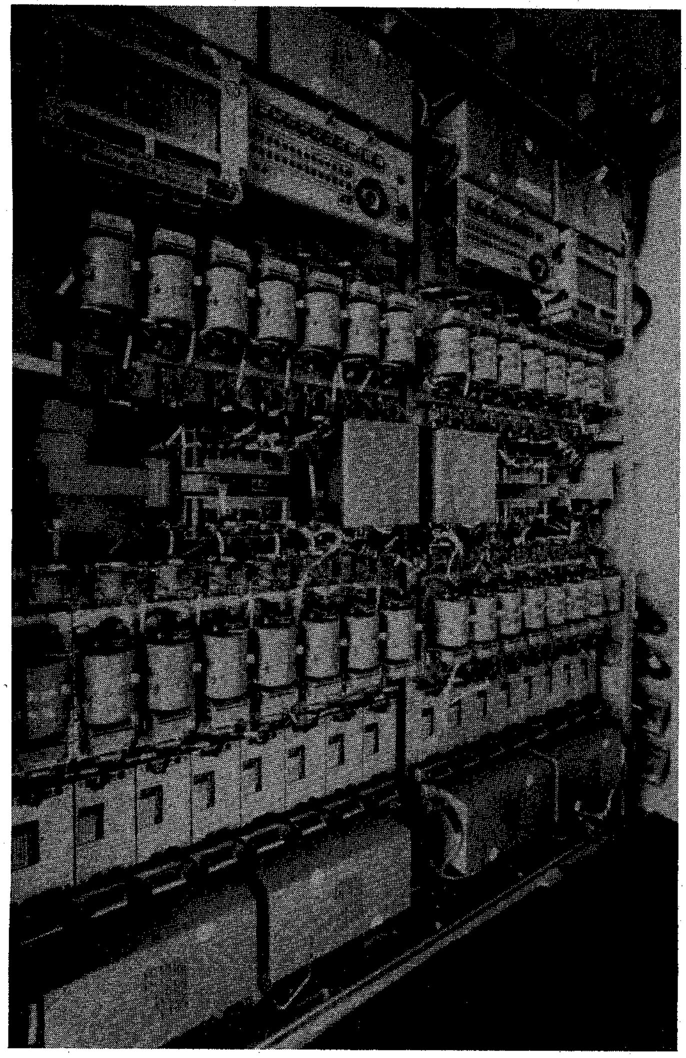

Fig. 9. Photograph of an AN/TPS-73 12 kW S-band solid-state transmitter.

ranged in four quadrants of 14 HPA's each. Each quadrant contains a cold plate for forced air cooling with the HPA's and voltage regulators mounted on both sides. The quadrants contain back-to-back 14 : 1 reactive, center-fed, suspended stripline divider and combiner networks in a radial configuration. The output from two quadrants (3.5 kW each) are combined (also back-to-back), in a waveguide magic T, via direct coupled probes from the 14 : 1 stripline combiner networks. This unique packaging concept results in a compact, very efficient, 28 : 1 combining network. The outputs from the magic T's on each side of the SST assembly feeds a rotary joint that permits the right- and left-side upper and lower cold plates and components to be rotated outward providing accessibility to the HPA and regulators on the back side. The HPA's are connected to the 14 : 1 divider/combiner by phase-matched flexible cables and coaxial junction circulators.

Also mounted on the cold plates are the power supplies, control electronics, RF switching and performance monitoring/fault isolation (PM/FI) circuits, and components.

TABLE III
12-kW SST Performance

Frequency	2.7 to 2.9 GHz
Pulse	100 μs and 10 μs
Duty cycle	10 percent
Output power	12 kW peak minimum
Input power	15.8 W peak
Gain	29 dB minimum
$\Delta P_o / \Delta V_{cc}$	0.2 dB/V
$\Delta \Phi / \Delta V_{cc}$	4.5°/V
V_{cc} regulation	3 mV
MTI improvement factor	>90 dB
Harmonic levels: (2nd, 3rd, and 4th)	80 dBc
Intrapulse stability:	< 1 dB amplitude droop < ±3° phase (linear)

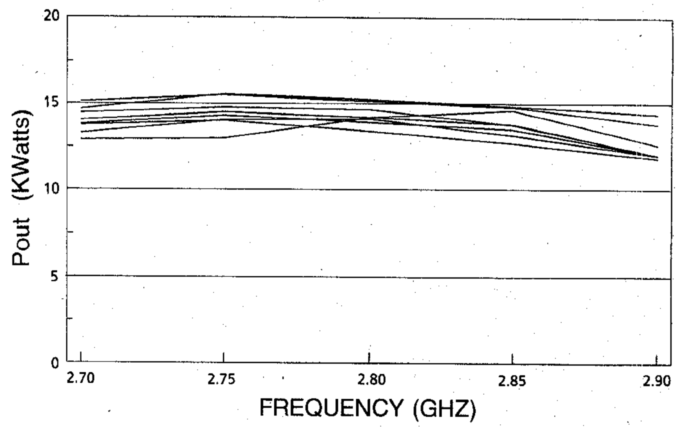

Fig. 10. Variation of output power of eight 12-kW SST's as a function of frequency.

Over-temperature protection is provided by thermocouples mounted in each of the cold plates.

The low-power amplifier (LPA) assembly is located on the back wall of the transmitter cabinet that contains the LPA's and a monitor detector used for low-power indication and VSWR protection.

VIII. Performance

The performance of the 12-kW SST is presented in Table III. The variation of output power as a function of frequency of representative production units are presented in Fig. 10. The instantaneous bandwidth of 200 MHz, output power of 12 kW, and required pulse fidelity are achieved. The MTI improvement factor of >75 dB for the 300-W HPA was measured. Based on the calculations shown in Section VI, the projected MTI improvement factor for the transmitter is >90 dB. At present, 18 MATACALS AN/TPS-73 12 kW solid-state transmitters have been produced.

IX. Conclusions

The design, fabrication, development and performance of a 12-kW solid-state transmitter (SST) for the Marine Corps, AN/TPS-73, has been demonstrated. This transmitter provides the enhanced performance required for new modern radars and for the upgrades of existing TWT/klystrons radar transmitters. This 12-kW MATCALS SST is in full-scale production and is operating at various locations around the world.

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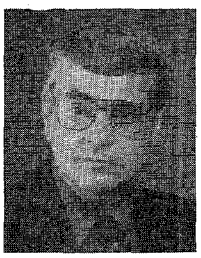
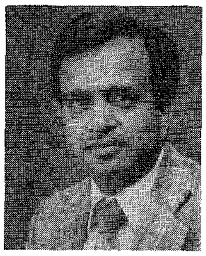


Michael Hanczor (S'69-M'72) was born in Yonkers, NY. He received the B.E.E. degree from Manhattan College, New York, in 1970 and the M.S.E.E. degree from the Polytechnic Institute of Brooklyn, New York, in 1974.

He is a Senior Project Engineer responsible for the development of solid-state high-power amplifiers and transmitters for the Unisys Government Systems Group Microwave Engineering Department. He has been employed at Paramax (A Unisys Company), formerly Sperry Corporation, for over 18 years, where he has been responsible for the design and development of microwave components and systems on such programs as artillery locating radar (ALR), Hemispheric Coverage Antenna (HCA), diamond antenna, advanced tactical radar (ATR), marine air traffic control and landing systems (MATCAL-SAN/TPS-73), and internal IR&D. Prior to joining Paramax, he was employed by Airborne Instruments Laboratory (AIL) and the Missile and Surface Radar Division of the RCA Corporation. At AIL, he was responsible for the design and development of low-noise parametric amplifiers, mixers, and receivers for space reconnaissance programs. At RCA, he was responsible for the development of the antenna radiating element for the AEGIS SPY-ID phased array antenna. He is the author of several technical papers on parametric amplifiers, low-noise receivers, solid-state high-power amplifiers, and transmitters.

Mr. Hanczor is presently co-program chairman for the Long Island Section of the IEEE MTT Chapter.



Mahesh Kumar (S'75-M'77-SM'83) received the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, India, in 1977.

From 1976 to 1978, he was a lecturer with Radar and Communications Center, Indian Institute of Technology, Kharagpur, India. From 1978 to 1985, he was employed by the RCA David Sarnoff Research Center, Princeton, NJ, where he conducted research and development work on GaAs MIC's and MMIC's. From 1985 to 1988, he worked for Microwave Semiconductor Corporation, Somerset, NJ, where he was responsible for the development of GaAs MMIC components, internally matched FET's and GaAs MMIC foundry. From 1988 to 1991, he worked for the AEL Defense Corporation, Landsdale, PA, where he was responsible for the development of microwave and millimeter wave circuits using MIC and MMIC technologies for transmitter and receiver applications. Since 1991, he has been with Unisys Government Systems Group, Great Neck, NY, where he is involved in the development of high-power amplifiers, and transmit/receive modules using Si and GaAs technologies.

Dr. Kumar is the author or coauthor of 50 journal and conference papers, the author of two book chapters, and holds 17 patents. He is a member of steering and technical program committee of the IEEE Microwave and Millimeter Wave Monolithic Circuits Symposium. He is also the past chairman of the IEEE Princeton section.